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Joining microelectronics and microionics: Nerve cells and brain tissue on semiconductor chips

Peter Fromherz *

Department of Membrane and Neurophysics, Max Planck Institute for Biochemistry, Martinsried, München, Germany

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ABSTRACT

The direct electrical interfacing of semiconductor chips with individual nerve cells and with brain tissue is considered. At first, the structure of the cell–chip contact is described and then the electrical coupling is characterized between ion channels, the electrical elements of nerve cells, and transistors and capacitors of silicon chips. On that basis, the signal transmission between microelectronics and microionics is implemented in both directions. Simple hybrid systems are assembled with neuron pairs and with small neuronal networks. Finally, the interfacing with capacitors and transistors is extended to brain tissue on silicon. The application of CMOS chips with capacitively coupled recording sites allows an imaging of neuronal activity with high spatiotemporal resolution. Goal of the work is an integration of neuronal network dynamics and digital electronics on a microscopic level for applications in brain research, medical prosthetics and information technology.

1. Introduction

Computers and brains work electrically. However, their charge carriers are different, electrons in solid silicon and ions in liquid water. It is an intellectual and technological challenge to join these different systems right on the level of their electronic and ionic signals. In principle, Luigi Galvani has established an electrical coupling between inorganic solids and excitable living tissue in the 18th century. Today, after fifty years of dramatic developments in semiconductor technology as well as in cellular neurobiology, we may envisage a most complex integration of microionics and microelectronics with myriads of nerve cells and semiconductor devices and breathtaking applications in medicine and information technology.

Usually, in neurophysiology the coupling of electronic and ionic signals is achieved with perfectly unpolarized solid/water contacts such as Ag/AgCl electrodes where ionic and electronic currents are transformed into each other. That approach is not suitable for an iono-electronic interfacing on a microscopic scale with numerous contacts. Semiconductor chips must be protected from corrosion, nerve cells from electrochemical reaction products. Interfacing must be implemented without Faradaic current. The communication between microionics and microelectronics must be achieved by displacement currents across an insulating interface [1,2].

The present paper describes step by step the mechanism of neuroelectronic interfacing on the scale of nanometers, micrometers and millimeters. It starts with the contact between an individual nerve cell and a silicon chip. Then the interfacing of the fundamental devices of the brain and the fundamental devices of computers is studied. On that basis, the interfacing of nerve cells with capacitors and transistors and the assembly of simple neuroelectronic hybrids with two nerve cells and with simple neuronal networks is considered. Finally, the challenges with electronic interfacing of brain tissue are addressed.

2. Cell–chip contact

A simple hybrid with a nerve cell from rat brain and a sensor transistor in silicon is depicted in Fig. 1. The cell is surrounded by a membrane with an electrically insulating core of lipid. That lipid bilayer (thickness about 5 nm) separates the bath with a concentration of 150 mM sodium ions from the cytoplasm with about 150 mM potassium ions. The silicon is coated with thermally grown silicon dioxide (thickness 10 nm). The basic problem with respect to the electrical interaction of cell and chip is the structure of the contact between the lipid bilayer and the oxide: What is the distance? (ii) What is the electrical resistance inbetween?

2.1. Distance

Silicon reflects light such that standing waves of the electromagnetic field are formed in front of its surface. We take advantage of that effect to measure the distance of cells and silicon using fluorescent dye molecules as antennas [3–5]. For that purpose, silicon chips are fabricated with microscopic oxide terraces (2.5 μm × 2.5 μm, step height about 20 nm). Cells are cultured on these substrates. The terraces of defined height together with the

* Tel.: +49 89 8578 2820; fax: +49 898578 2822.
E-mail address: fromherz@biochem.mpg.de.

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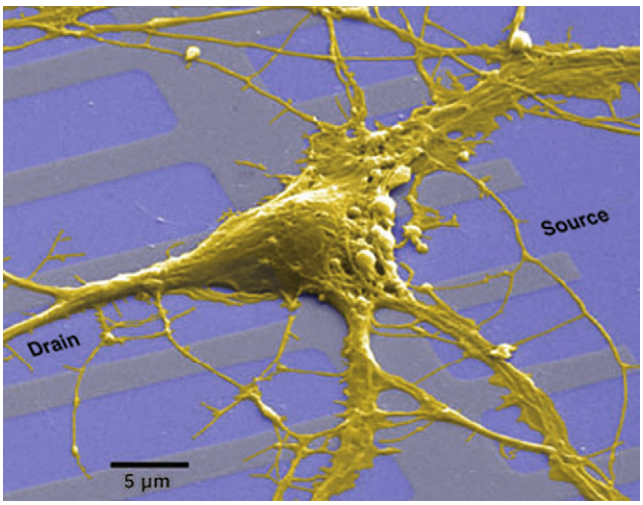

Fig. 1. Nerve cell from rat brain on silicon chip. Electronmicrograph after fixation. The surface of the chip consists of thermally grown silicon dioxide. The metalfree gates of a linear array of low-noise field-effect transistors are visible as bright squares between the dark regions of sources and drains. The neuron is cultured for several days in electrolyte.

unknown distance between chip and cell bring the cell membrane into different positions in the standing light waves. The lipid bilayer of the cell membrane is labeled with a fluorescent dye. When we evaluate the measured fluorescence intensities on a set of terraces with the classical antenna theory, we find that there is a cleft between the oxide and the lipid bilayer. Results for rat neurons on chips coated with polylysine [6] are plotted in Fig. 2a with an average distance around 50 nm.

2.2. Resistance

The electrical coupling of chip and cell depends on the resistance of the 50 nm cleft between oxide and membrane. To measure the sheet resistance we apply an alternating voltage to the chip. The resistance of the cleft together with the capacitances of oxide and membrane determines the phase of the alternating voltage that is induced across the membrane. We probe the phase shift with a fluorescent dye that exhibits a molecular Stark effect [7,8]. The phase map of the fluorescence intensity is evaluated in terms of a two-dimensional core-coat conductor. The sheet resistance of the cleft is shown in Fig. 2b for rat neurons on polylysine [6] with an average around 10 MΩ square. When we combine the resistance measurement with the distance measurement, we find that the 50 nm cleft is filled with bulk electrolyte from the surrounding bath.

The thin film of electrolyte between oxide and membrane prevents a direct electrostatic polarization of a cell from a chip and of a chip from a cell, respectively.

3. Ion–electron coupling

The electrical elements of nerve cells are voltage-gated ion channels. These molecules are embedded in the lipid bilayer of the membrane. They can be in an open and in a closed state. When they are open, they selectively transmit ionic current through the membrane, Na^+ inward current or K^+ outward current. The opening and closing of the channels is connected with a displacement of electrical charge across the membrane. As a consequence, opening and closing can be controlled by the voltage across the membrane.

The electrical communication between semiconductors and cells must rely on an interaction of the ion channels with the chip. Two devices are used, electrolyte/oxide/semiconductor (EOS) capacitors for the activation of the channels and electrolyte/oxide/semiconductor (EOS) field-effect transistors for the detection of open channels. The interaction of channels and chips is determined by the electrical nature of the cell–chip contact with the insulating oxide, the insulating lipid bilayer and the thin film of electrolyte in between (Fig. 3).

3.1. EOS capacitors and ion channels

We test the electrical signaling from chip to cell with HEK293 cells that are transfected with the gene of the potassium channel Kv1.3. The cells are cultured on an EOS capacitor. A falling voltage ramp is applied to the capacitor (Fig. 3a). A displacement current flows across the oxide and gives rise to an ohmic current along the sheet resistance of the cell–chip contact. The resulting negative extracellular voltage opens the channels in the attached membrane.

To achieve a sufficiently high displacement current, the silicon chip is insulated by titanium dioxide with a high dielectric constant [9]. In addition a bath electrolyte with an enhanced resistivity is used. The ion current through the membrane is measured with a micropipette that is fused to the cell membrane. The experiment is performed at a constant intracellular voltage where the channels are closed without capacitive stimulation. An example is shown in Fig. 4. During falling voltage ramps, the current through the membrane is enhanced, depending on the slope of the ramp [10].

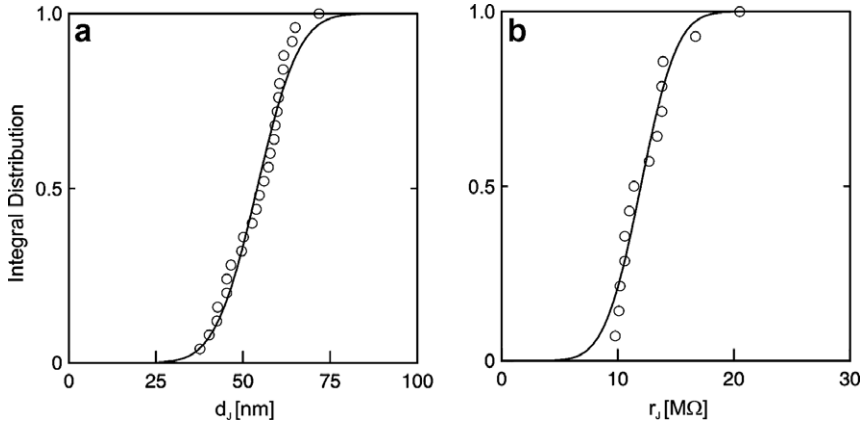

Fig. 2. Contact between nerve cell and silicon chip coated with polylysine. (a) Integral distribution function of the distance between the lipid bilayer of the cell membrane and the oxide of the chip. (b) Integral distribution function of the electrical sheet resistance of the cleft between cell and chip.

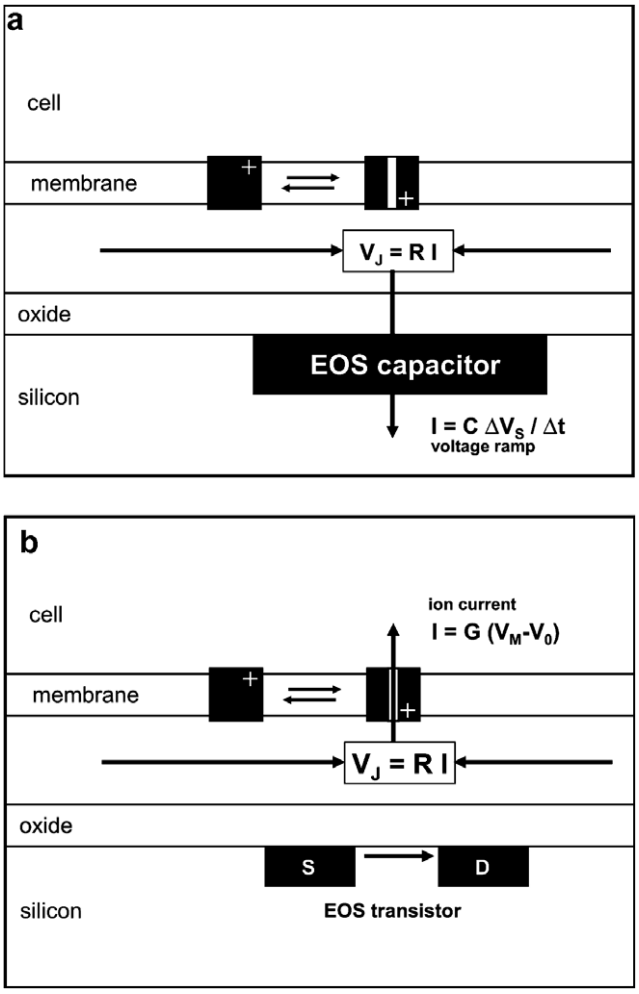

Fig. 3. Ionoelectronic interfacing on the basis of Ohm's law. (a) Activation of voltage-gated ion channels by an electrolyte/oxide/semiconductor (EOS) capacitor. A falling voltage ramp is applied to the chip: the displacement current across the oxide gives rise to a negative extracellular voltage V_J that opens the channels. (b) Recording of ion channels by an EOS field-effect transistor. Inward ion current through open channels gives rise to a negative extracellular voltage V_J such that the electronic current in a field-effect transistor is modulated.

The current signal is specific for Kv1.3 channels as proven by the application of a selective toxin.

The experiment shows that the ionic current in the cell is controlled by an electronic signal in the semiconductor. Consider the current–voltage–current mechanism: A displacement current across the oxide is transformed to an extracellular voltage between oxide and membrane that induces an ion current through the membrane.

3.2. EOS FETs and ion channels

We test the signaling from cells to chips with HEK293 cells that are transfected with the gene of the sodium channel Nav1.4. The cells are cultured on an EOSFET (Fig. 3b). The thin electrolyte film between cell and chip plays the role of a gate. Using a micropipette, positive voltage pulses are applied to the cell to open the channels. Na^+ current flows into the cell and along the sheet resistance of the cell–chip contact. It gives rise to a negative extracellular voltage that modulates the electron current from source to drain [11].

We simultaneously record the transistor signal as well as the total membrane current using the micropipette as shown in Fig. 5.

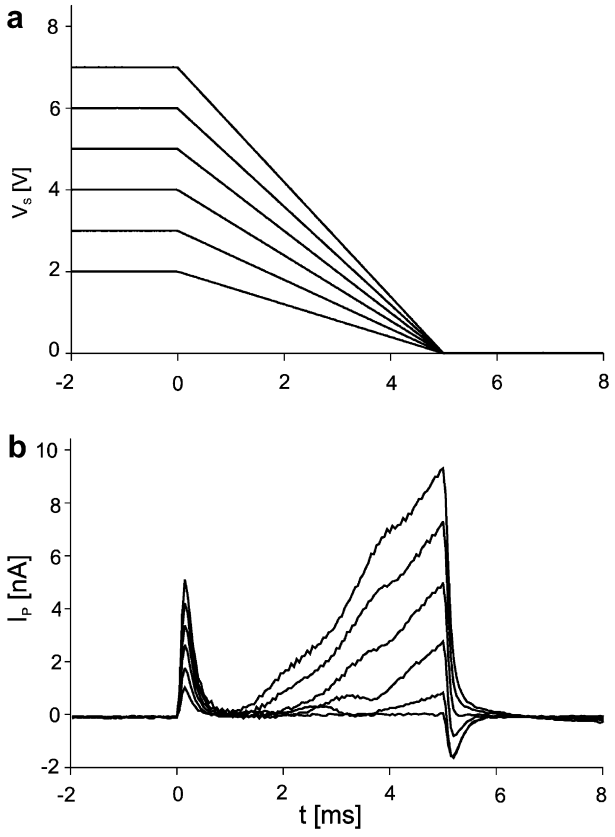

Fig. 4. Capacitive activation of potassium channels. HEK293 cells with recombinant Kv1.3 channels are cultured on a electrolyte/TiO_2/silicon capacitor. The intracellular voltage is kept constant with a patch pipette. (a) Falling voltage ramps applied to the chip. (b) Membrane current across the attached membrane during the ramps.

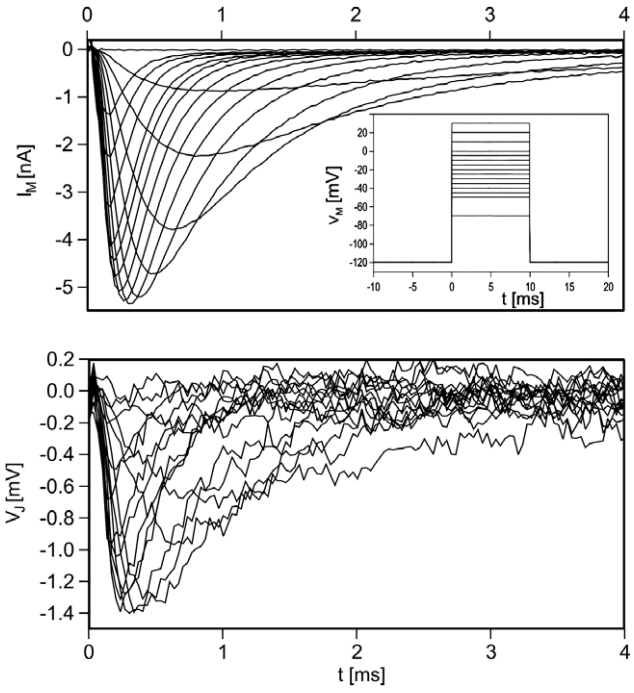

Fig. 5. EOSFET record of sodium channels. HEK293 cells with recombinant Nav1.4 channels are cultured on a electrolyte/SiO_2/silicon field-effect transistor. Positive voltage pulses are applied to the cell (inset). (a) The transient membrane currents indicate open sodium channels. (b) The EOSFET responds to the transients of the extracellular voltage that are proportional to the membrane current.

When positive voltage pulses are applied to the cell, a typical transient inward current is observed through the membrane. Simultaneously, a transient transistor signal appears that has a similar waveform. A quantitative evaluation shows that the transistor voltage is proportional to the membrane current as determined by the resistance of the cell–chip contact.

The experiment demonstrates that the electronic current in the semiconductor is controlled by the ionic signal in the cell. Note again a current–voltage–current mechanism: An ion current through the membrane is transformed into an extracellular voltage between oxide and membrane that modulates the electron current in the semiconductor.

4. Semiconductor chips with nerve cells

A first step towards an integration of neuronal dynamics and microelectronics is the interfacing of individual nerve cells with silicon microstructures. We consider the excitation of nerve cells by EOS capacitors and the recording of neuronal activity by EOSFETs.

A crucial issue is the contribution of two domains of a nerve cell, the membrane that is attached to the chip and the upper free membrane in contact to the bath as illustrated in Fig. 6: (i) When a voltage ramp is applied to a capacitor, the extracellular voltage in the cleft between chip and cell polarizes the attached membrane as well as the upper membrane in opposite directions. Ion channels may be affected in both domains. (ii) When a nerve cell is excited, there are ion currents through the attached as well as through the upper free membrane that determine the change of intracellular voltage during an action potential. Only the current through the attached membrane gives rise to an extracellular voltage modulating the transistor. It has an ionic component due to the channels in the attached membrane and a capacitive component that depends on the total ion current through the attached and free membrane.

4.1. EOS capacitor stimulation

We dissociate nerve cells from the ganglia of pond snails and attach them to a stimulation capacitor. Rising and falling voltage ramps are applied and the intracellular voltage is recorded with a micropipette as depicted in Fig. 7 [12]. A rising voltage ramp leads to a positive extracellular voltage between chip and cell.

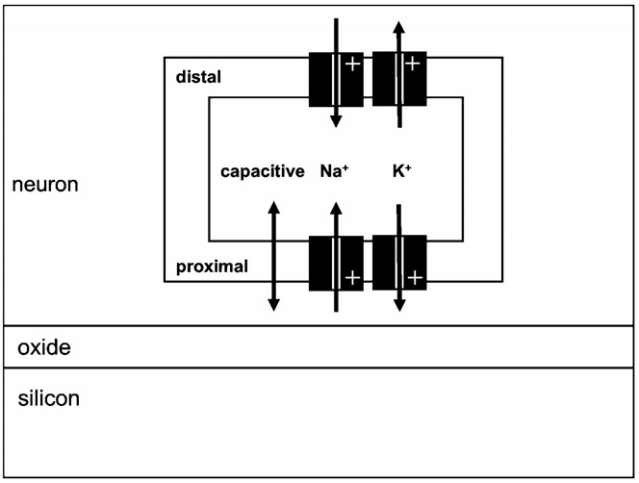

Fig. 6. Scheme of a nerve cell on a silicon chip. The current through various kinds of ion channels and the capacitive current must be considered through the attached (proximal) membrane and through the free upper (distal) membrane for stimulation with an EOS capacitor as well as for recording with an EOSFET.

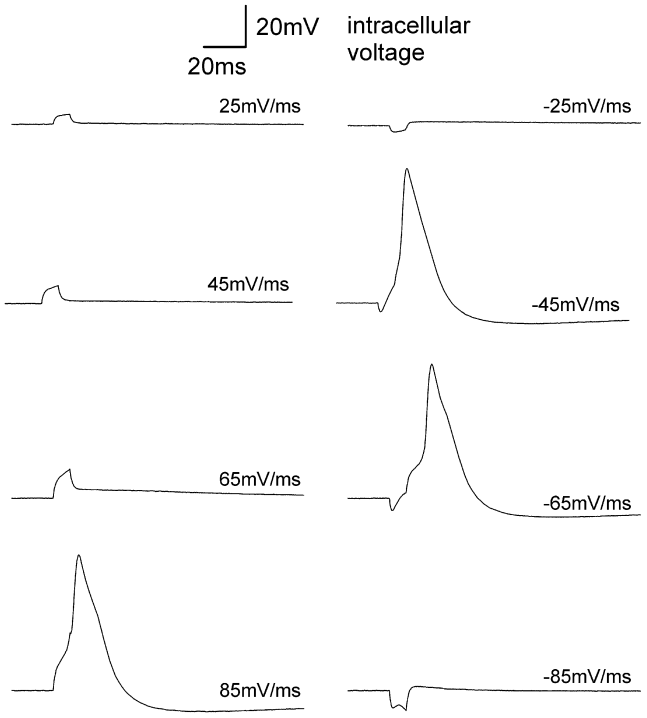

Fig. 7. Capacitor stimulation of snail neuron. Response of intracellular voltage to rising and falling voltage ramps applied to an EOS capacitor. Left: rising voltage ramps with increasing slope as indicated. Right: falling voltage ramps with increasing slope.

The voltage drop across the upper membrane gives rise to an activation of Na^+ channels in the upper membrane such that an action potential is elicited above a certain threshold as shown in Fig. 7a. A rather high slope of the ramp is required because most of the extracellular voltage drops across the attached membrane with its small area. When a falling voltage ramp is applied, a negative extracellular voltage is induced between chip and cell. Na^+ channels are activated there. The resulting inward Na^+ current depolarizes the whole cell membrane such that an action potential is elicited as shown in Fig. 7b. That effect disappears for strong stimuli when an outward K^+ current is activated, too.

4.2. EOS FET recording

Nerve cells from the ganglia of leech are placed on electrolyte–oxide–silicon field-effect transistors. They are impaled with a micropipette electrode for stimulation and for recording the intracellular voltage. The calibrated sensor transistors detect the transient extracellular voltage between cell and chip. Two examples are shown in Fig. 8 [13,14]. In the first record, the extracellular voltage shows a peak in the rising phase of the intracellular voltage and a trough in its falling phase. In the second experiment, the transistor signal shows a trough in the rising phase and a peak in the falling phase. The different signals reflect different contributions of ionic and capacitive currents through the attached cell membrane. The first signal is dominated by the capacitive current through the attached membrane that is driven by ionic currents through the upper free membrane. The second record is determined by the ionic currents in the attached membrane itself with a sharp Na^+ inward current and a delayed K^+ outward current.

The different types of neuronal recordings indicate that the ion channels are inhomogeneously distributed in the cell membrane and that the cells are differently attached to the transistor in the two experiments. That interpretation is tested when the neuronal

excitation is not probed with a single transistor, but with a closely packed array of sensor sites that are derived from the EOSFET principle. Such an array is fabricated by using an extended CMOS technology [15]. Fig. 9 shows cultured snail neurons on the surface of a CMOS chip with 16,384 sensor sites on 1 square mm. When a selected nerve cell is excited with a micropipette, a set of sensor sites beneath the cell is able to map the extracellular voltage in the cell–chip contact [16]. Different waveforms of the extracellular voltage are observed for different positions beneath a single nerve cell (Fig. 10). Thus neuroelectronic interfacing depends on structural details of the cell–chip contact.

With small nerve cells from mammalian brains, we expect far smaller extracellular voltages during an action potential than for the large neurons from leech and snail. Successful recordings are achieved with buried-channel transistors [17]. The response of a linear transistor array to a firing neuron is shown in Fig. 11 with amplitudes of about 200 μV [18].

It is important to note that the background noise of transistors that are covered by the cell is larger than the noise of the free transistors. That effect is due to the Nyquist noise of the cleft resistance between cell and chip. In the frequency range of the action potentials, the power density of that thermal noise is similar to the intrinsic 1/f noise of the transistor. It sets a thermodynamic limit for the signal-to-noise ratio of neuroelectronic interfacing.

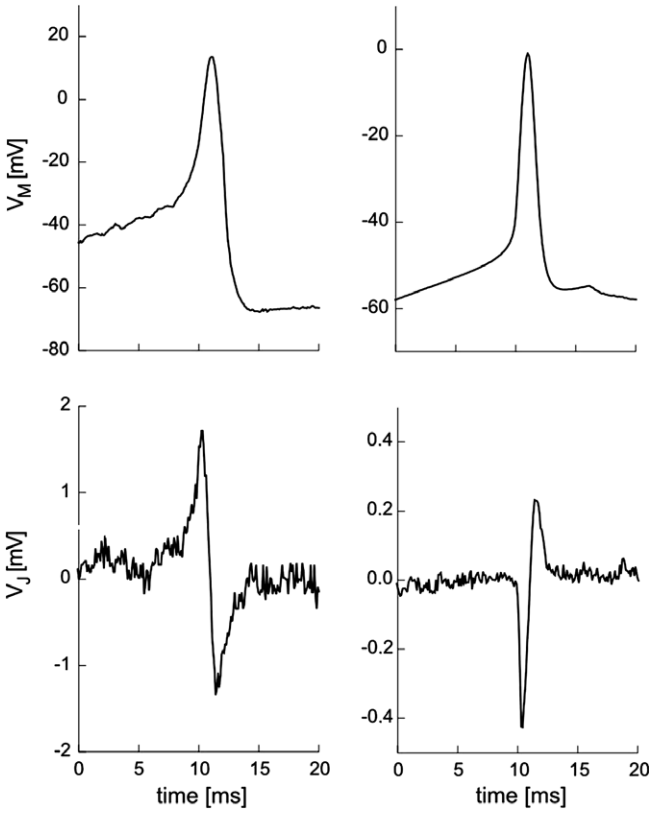

Fig. 8. Transistor records of leech neurons. The upper row shows the intracellular voltage during an action potential, the lower row the extracellular voltage measured with an EOSFET. Left: the transistor signal is dominated by the capacitive current across the attached membrane. Right: the transistor signal is due to sodium and potassium currents across the attached membrane.

Fig. 10. Simultaneous records at different positions of the same excited snail neuron. Top trace: intracellular voltage with three action potentials. Lower traces: records of three sensor transistors of CMOS chip with different waveforms.

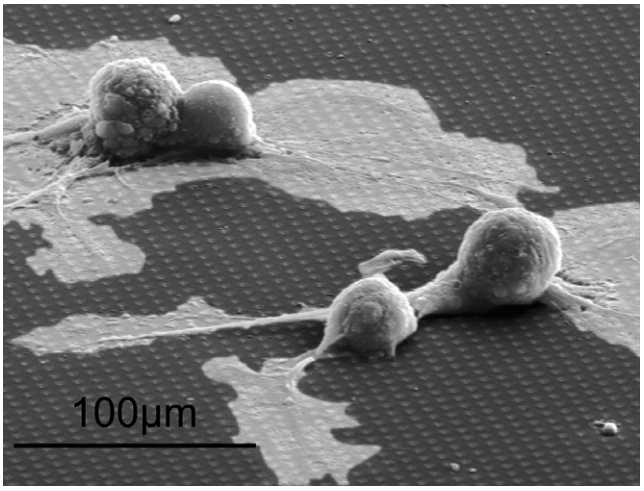

Fig. 9. Nerve cells from pond snail on the array of sensor transistors of a CMOS chip. Electronmicrograph. The contacts of recording sites (16,384 on 1 square mm) shine through the surface layer of the chip made of TiO_2. The sensor array allows a mapping of extracellular voltage beneath individual nerve cells with a resolution of 7.8 μm.

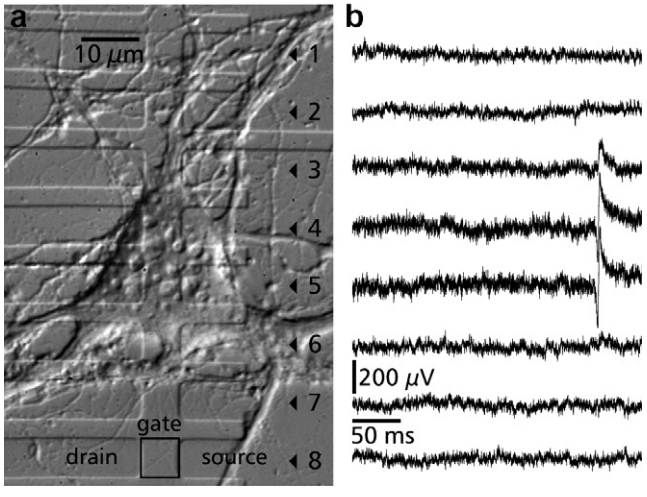

Fig. 11. Transistor recording of rat neuron. (a) Micrograph of nerve cell on a linear array of EOSFETs. The elements of a selected transistor are indicated at the bottom. The cell body completely covers the gates Nos. 4 and 5. (b) Extracellular voltage recorded by the transistors within a bandwidth of 1 Hz to 10 kHz. The transistors beneath the cell body exhibit an enhanced noise. Near the end of the traces, the transistors Nos. 3, 4, and 5 record spontaneous neuronal excitation.

5. Elementary neuroelectronic hybrids

In a first step towards the assembly of neuroelectronic hybrids, we couple pairs of nerve cells to a chip with two different pathways as illustrated in Fig. 12.

5.1. Cellular chip-prosthesis

A cellular neuroprosthesis is implemented as a "neuron–silicon–silicon–neuron" system where the activity of a neuron is recorded and used for stimulation of a second neuron after electronic processing on the chip [19]. Two snail neurons are attached to a silicon chip with EOS capacitor and with EOSFETs. They have no direct contact to each other (Fig. 13a). The spontaneous activity of the first neuron is recorded by the transistor. The record of an action potential is identified on the chip and elicits a digital signal. A delay line is triggered, and a burst of voltage pulses is created and applied to the capacitor such that neuronal activity is induced in the second neuron. A crucial problem in that system is the crosstalk from the stimulation EOS capacitor back to the EOSFET. Resulting artifacts of the transistor record must be eliminated on the chip.

5.2. Neuronal memory on chip

A neuronal memory element is obtained as a "silicon–neuron–neuron–silicon" system where a capacitively stimulated neuron is coupled to a second neuron through a chemical synapse and where the postsynaptic response is detected with a transistor [20]. Two identified snail neurons are attached to an array of EOS capacitors and EOSFETs such that they form a soma–soma contact with a chemical synapse (Fig. 13b). The presynaptic nerve cell is stimulated from a capacitor, the signal activates the chemical synapse and the postsynaptic excitation is recorded with an EOSFET. In a first test, there may be no postsynaptic activity if the synaptic coupling is weak. When a series of capacitive presynaptic stimuli is applied, the synaptic strength is enhanced such that a second test reveals a postsynaptic action potential that is recorded by the transistor. The two-neuron hybrid implements a neuronal memory on chip.

6. Neuronal networks on chip

The function of complex neuronal networks relies (i) on an ordered mapping between sets of neurons by synaptic connections and (ii) on an enhancement of the synaptic strength by correlated presynaptic and postsynaptic activity (Hebbian learning). An experimental study of that function requires (i) neuronal nets with a defined topology of the synaptic connections, and (ii) a noninvasive supervision of all neurons to induce learning and to observe the performance of the network. To achieve these goals we must control the neuronal outgrowth and the formation of synapses, and we must fabricate silicon chips with arrays of numerous two-way contacts.

6.1. Immobilized neurons

Neuronal networks can be obtained in cell culture from nerve cells that are dissociated from the brain of snails and rats. During

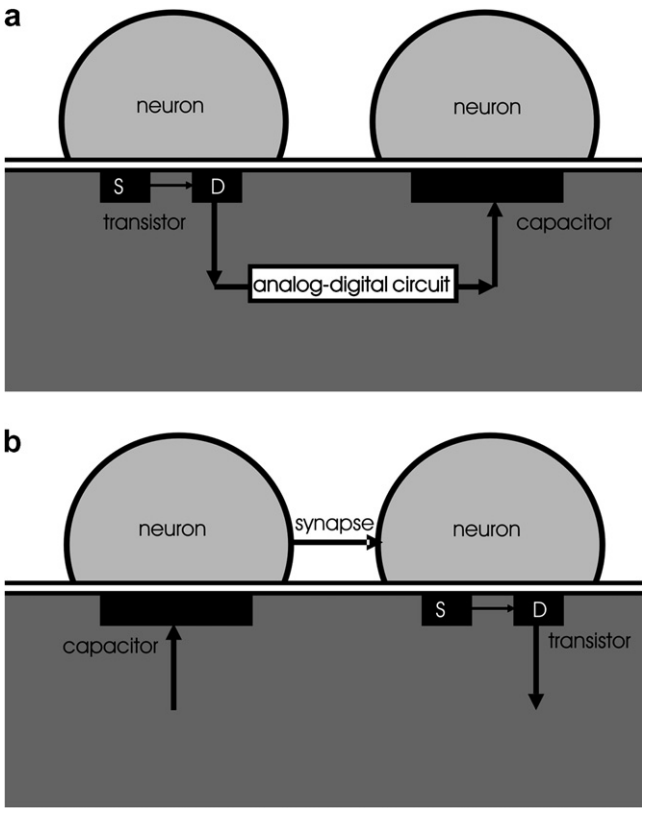

Fig. 12. Elementary neuroelectronic hybrids. (a) Cellular neuroprosthesis. An input neuron is probed by a transistor. The signal is processed on the chip and applied to a capacitor that stimulates an output neuron. (b) Neuronal memory on chip. An input neuron is stimulated from the chip and coupled by a synapse to an output neuron. The synaptic strength is potentiated by capacitive stimulation.

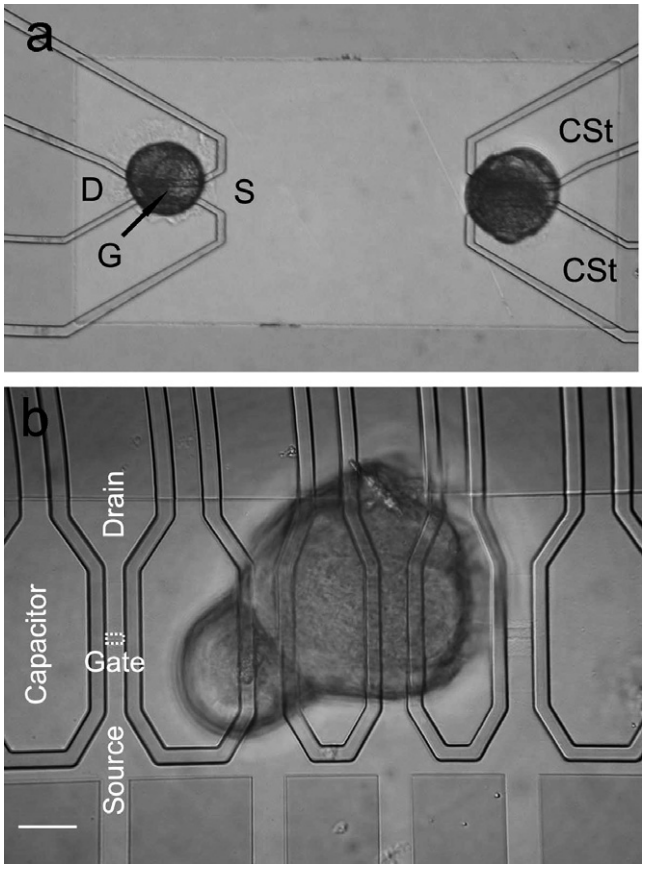

Fig. 13. Implementation of elementary neuroelectronic hybrids. (a) Cellular neuroprosthesis with an input neuron (left) on an EOS transistor (D, G, S) and a separated output neuron (right) on an EOS capacitor (CSt). (b) Neuronal memory on a chip with an input neuron (small) on a capacitor, a synapse between the cell bodies and an output neuron (large) on an EOS transistor.

outgrowth, however, the cell bodies are displaced on the chip such that the junctions with sensor transistors and stimulation capacitors are disrupted. That displacement is caused by the forces of the growing neurites that tend to shorten in cell culture. To overcome that problem, picket fences of organic polymers are fabricated on chip and the neuronal cell bodies are mounted as shown in Fig. 14a [21]. The cell bodies are perfectly kept on the two-way contacts made of stimulation capacitors and sensor transistors, even after culturing for several days. In such a system, a selected neuron is excited by a capacitor, a postsynaptic action potential is elicited through electrical synapses and the signal is recorded with a transistor.

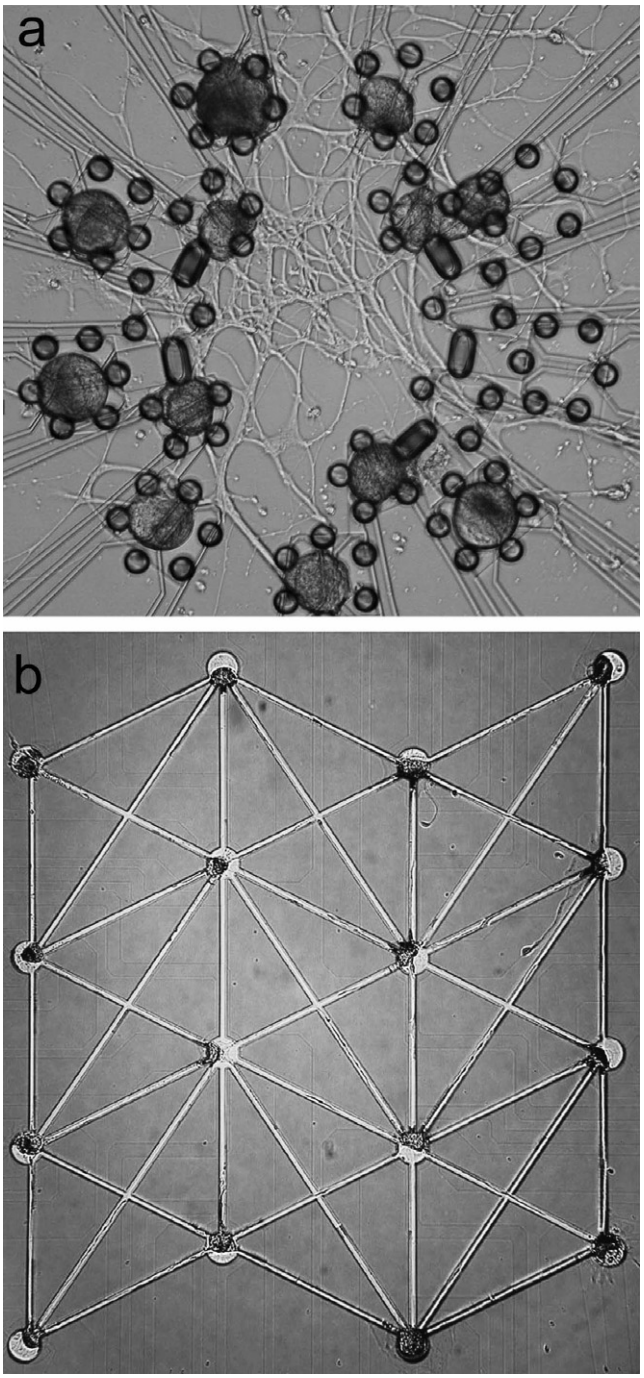

Fig. 14. Neuronal networks on silicon chip. (a) Mechanical immobilization of cell bodies (dark blobs) by picket fences of an organic polymer (small dots) on capacitor/transistor contacts with neurites grown in the central area (bright threads). (b) Mechanical immobilization of the cell bodies by wells on 16 capacitor/transistor contacts and of grown neurites by guiding grooves in a organic polymer.

6.2. Topographical guidance

The outgrowth of neurons can be controlled by chemical patterns. However, that kind of guidance is not stable due to the strong contracting forces of growing neurites. Topographical guidance may overcome that problem. An example is shown in Fig. 14b. Using an organic polymer, wells and connecting grooves are fabricated on a chip with 16 two-way contacts of stimulation capacitors and sensor transistors. After placing snail neurons into the wells, their outgrowth is guided by the grooves such that electrical synapses are formed [22]. In principle, it is possible to create defined neuronal networks that are supervised from a chip. However, at present the overall yield is too low to implement complex systems.

6.3. Random nets on CMOS chips

The problem of displaced neurons is bypassed when an array of closely packed EOS capacitors and recording transistors is used, such that a displaced neuron finds itself on one or more two-contact sites, wherever it is on the chip. Of course, the defined control of network geometry is sacrificed in such systems. However, when the changing geometry is continuously monitored by the chip, we may perform experiments with complex patterns of stimulation that induce a spatially distributed neuronal memory on chip.

6.4. Synaptic recording

In order to supervise a neuronal network, it is important not only to record the activity of all presynaptic and postsynaptic neurons, but also the activity of all synapses. In a first step towards that ambitious goal, we use chromaffin cells from the adrenal gland as a model for the presnaptic release of vesicles [23]. The cells are attached to EOSFETs (Fig. 15a). A carbon fiber is used for electrochemical recording of vesicle release. Upon chemical stimulation, a burst of events is recorded with the transistor simultaneously with a response of the carbon fiber (Fig. 15b). In that system, the EOS transistors work as ion sensitive devices that record the local pH change that is caused by the vesicles. Whether that approach can be used to record neuronal synapses with their far smaller vesicles has to be studied.

7. Semiconductor chips with brain tissue

Culturing of defined neuronal networks can be avoided when neuronal networks are used that are provided by brains. Brain tissue with a planar structure of the networks is required to attain an efficient interfacing with a planar chip. Organotypic brain slices are particularly promising because they are a few cell layers thick and conserve major neuronal connections. Compared to the culture of dissociated cells, however, there are new problems if we want to interface individual nerve cells in a tissue: (i) we cannot take it for granted that individual nerve cells are attached to individual stimulation capacitors and sensor transistors with a distance of 50 nm. (ii) There are so many neuronal cell bodies embedded in glia cells and in a web of dendrites and axons, that we do not know which cell is coupled to a particular stimulation or recording site. It will be an important task to investigate the structural and electrical features of the tissue-chip contact with similar optical methods as used for cultured cells.

In a first approach, we attempt to achieve an electrical interfacing of organotypic brain slices on the level of neuronal groups, i.e. we stimulate a small area of presynaptic brain tissue with an EOS

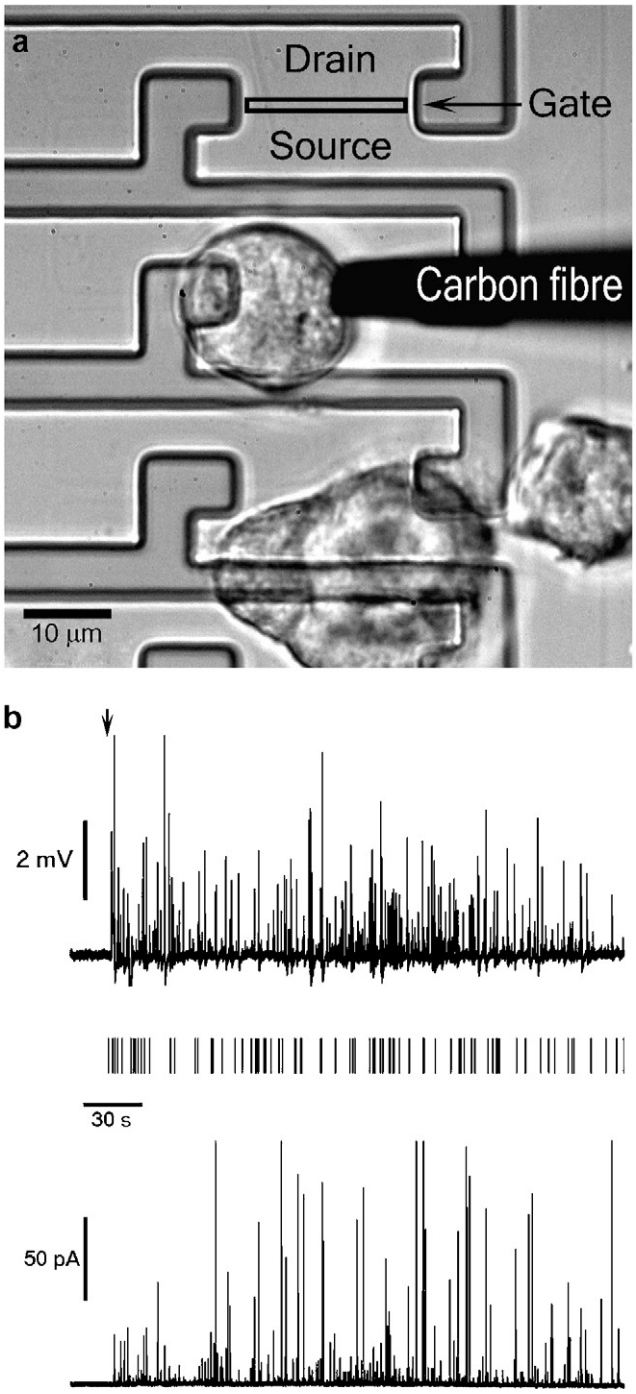

Fig. 15. Chromaffin cell on transistor as a model of synapse recording. (a) Micrograph with linear array of EOSFETs. Source, drain, and gate (black frame) are marked on an upper transistor. A chromaffin cell covers about one half of an open gate (2 μm × 20 μm). The cell is touched by a carbon fiber from the right. (b) Simultaneous detection of vesicle release by EOSFET (top) and amperometry (bottom). The stimulation by 5 mM $BaCl_2$ is marked by an arrow. The vertical bars between the two records mark the events that are detected by transistor and carbon fiber within a window of 5 ms.

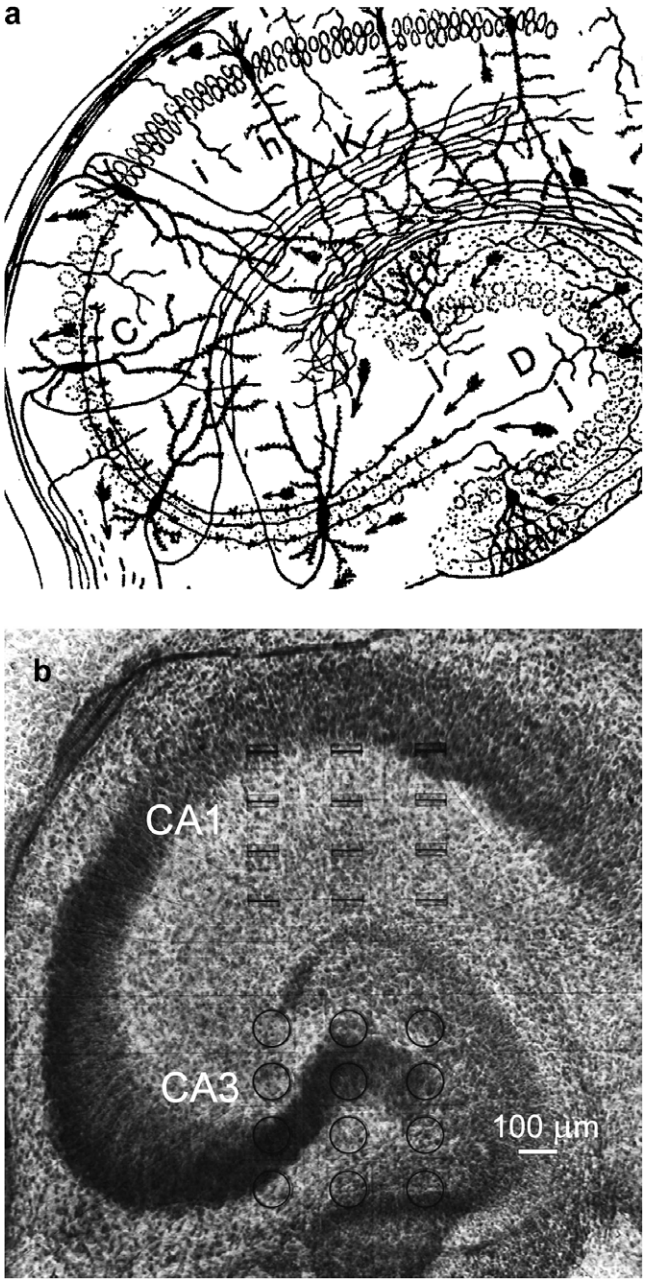

Fig. 16. Rat hippocampus on silicon chip. (a) Transverse section of hippocampus that shows the neuronal wiring (Ramon y Cajal, Golgi stain). (b) Hippocampus slice (Nissl stain) cultured on a chip with an array of large stimulation EOS capacitors (circles) and an array of large EOSFETs (bars).

capacitor and detect the average postsynaptic activity in another small area of tissue with an EOSFET [24,25].

7.1. Two-way interfacing of slices

Fig. 16a shows a classical picture of the wiring in a transverse section of rat hippocampus. We place a slice on a chip with an array of large stimulation capacitors and an array of large sensor transistors as shown in Fig. 16b. The capacitors are in the CA3 region whereas the transistors are in the CA1 region of the hippocampus. These two areas are connected by axons (Schaffer collaterals). When the CA3 regions is stimulated, excitatory synapses in the CA1 regions are activated.

In fact we are able to stimulate the cell bodies of CA3 with sharp falling voltage ramps applied to a capacitor and to record with a certain delay extracellular voltages in the region of CA1 as shown in Fig. 17. The postsynaptic signal appears above a threshold of the capacitive stimulus when neurons are excited above the center of the capacitor [25]. An enhanced stimulus leads to an expansion of the area where presynaptic neurons are excited such that more postsynaptic neurons are activated with increasing amplitude of the postsynaptic signal.

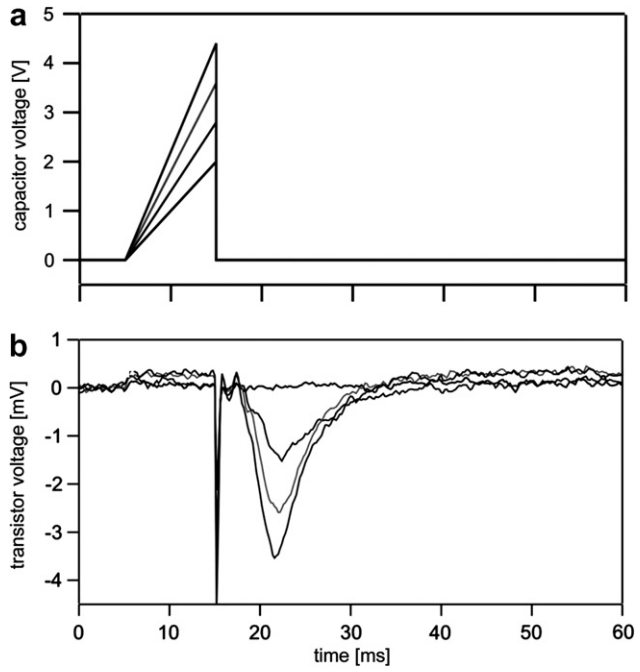

Fig. 17. Capacitor stimulation and transistor recording of hippocampus slice. (a) Falling voltage steps are applied to an EOS capacitor in the CA3 region. (b) Extracellular postsynaptic voltages are recorded by an EOSFET in the CA1 region.

7.2. Slice mapping with CMOS chip

Interfacing of brain tissue with cellular resolution requires a high density of stimulation and recording sites. In a first approach, the mapping of postsynaptic activity is studied on the level of neuronal groups using a CMOS chip with 16,384 sensor transistors on 1 square mm.

Fig. 18a shows a chip with an organotypic hippocampus slice where the recording array covers the CA3 region. A tungsten electrode is used to stimulate axons that enter the CA3 region (mossy fibers). Fig. 18b shows the distribution of extracellular voltage 5 ms after stimulation [26]. We see a negative signal in the region of the dendrites (stratum radiatum) and a positive signal in the region of the cell bodies (stratum pyramidale). The action potential in the presynaptic axons activate the synapses in the dendritic region where current flows into the cells such that a negative extracellular voltage is created. The compensating outward current leads to positive voltage in the region of the cell bodies. The CMOS chip provides a time resolved map of activity with a resolution of 2 kHz. Examples of the local dynamics are plotted in Fig. 19 that show the excitatory postsynaptic synaptic potentials (EPSP) and the superposed action potential of postsynaptic neurons (population spike).

The experiments are first steps towards a complete interfacing of brain tissue on the level of individual neurons in both directions. Given the features of the hippocampus, we can envisage far reaching experiments on an associative neuronal memory that is integrated with a semiconductor chip.

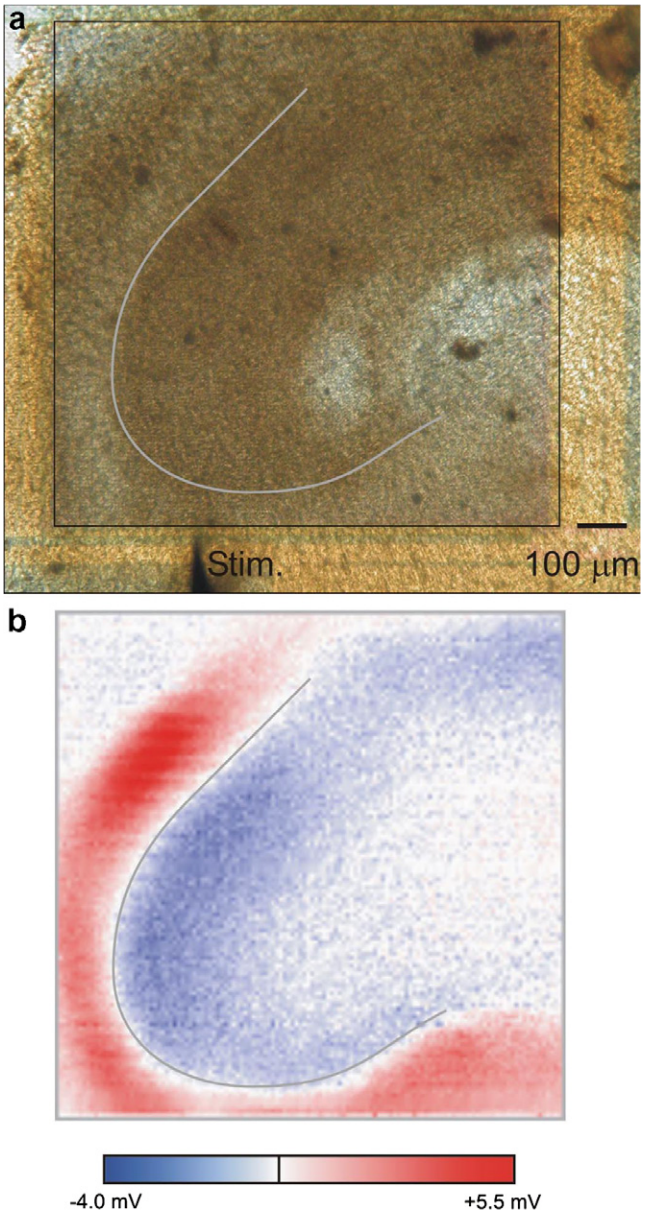

Fig. 18. Functional mapping of brain slice activity by multitransistor array (MTA) recording. (a) Cultured hippocampus slice. The square marks the area of 16,384 sensor sites on 1 square mm. The slice is stimulated by a tungsten electrode at the bottom (Stim). The bent line is redrawn from the activity map below. (b) Extracellular voltage 5 ms after stimulation: activity of synapses in the area of inward current (negative within bent line) and compensating outward current (positive beyond bent line).

8. Outlook

The basic problems on the electrical interfacing of individual nerve cells and semiconductor chips are solved. Important progress was achieved by the development of stimulation EOS capacitors with high dielectric constant, of sensor EOS transistors with low-noise and of CMOS chips with a high density of sensor sites.

With respect to hybrid systems of neuronal networks and digital microelectronics, we are still in an elementary stage. Several directions may be considered: (i) small defined networks of neurons from invertebrates and mammals are created with defined topology and with learning synapses. (ii) Large random neuronal nets are grown on closely packed arrays of two-way contacts fabricated by CMOS technology. (iii) The interfacing of brain slices in both directions is established on the level of neuronal groups with large two-way arrays on CMOS chips. (iv) The structure of the chips is modified such that they can be applied to brains.

Of course, visionary dreams of bioelectronic neurocomputers and microelectronic neuroprostheses are unavoidable and exciting. However, they should not obscure the numerous practical problems that have to be solved.

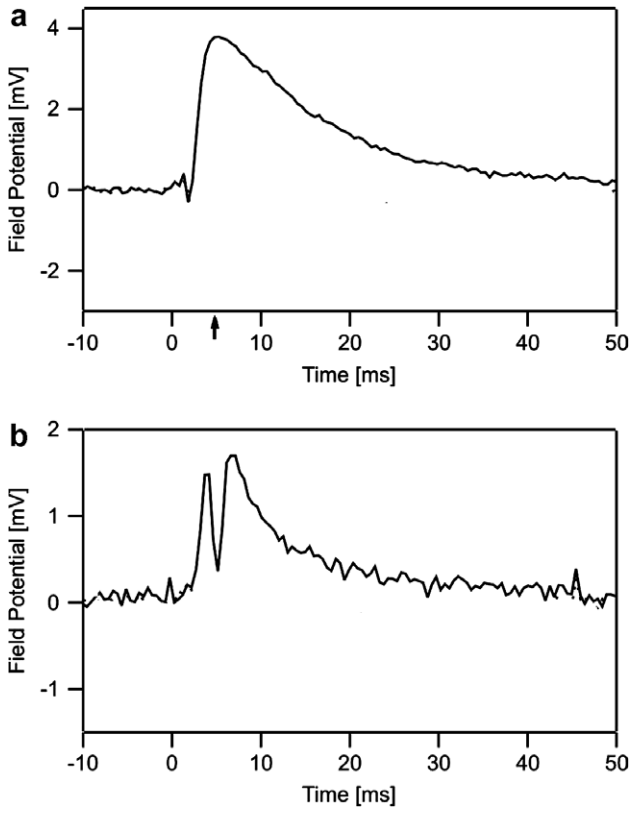

Fig. 19. Dynamics of the local extracellular voltage (field potential) probed with different sensor transistors of CMOS chip. (a) Record of excitatory postsynaptic synaptic potential (EPSP) in stratum pyramidale of CA3. (b) EPSP and superposed population spike in CA1.

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